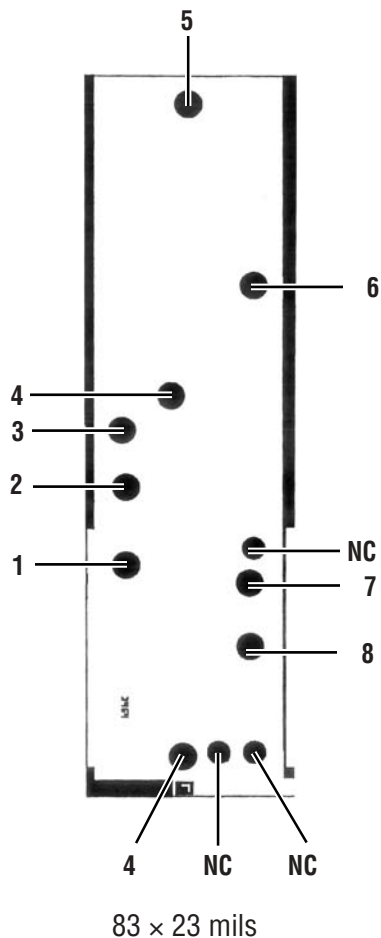


Micropower Boost Converter with
 Schottky and Output Disconnect in ThinSOT™

DIE CROSS REFERENCE

| LTC Finished Part Number | Order DICE CANDIDATE Part Number Below |
|--------------------------|--|
| LT3464 | LT3464 DWF |
| LT3464 | LT3464 DICE |

PAD FUNCTION

1. CTRL
2. FB
3. OUT
4. GND
5. CAP
6. SW
7. V_{IN}
8. SHDN

12mils thick,
 backside (substrate) is an alloyed
 gold layer. Connect backside to V^- .

ABSOLUTE MAXIMUM RATINGS

(Note 1)

| | |
|-------------------------------------|-----|
| V_{IN} , SHDN, CTRL Voltage | 10V |
| OUT, CAP Voltage | 36V |
| SW Voltage | 36V |
| FB Voltage | 6V |

DICE/DWF SPECIFICATION

LT3464

DICE ELECTRICAL TEST LIMITS $T_A = 25^\circ\text{C}$. $V_{IN} = 3.6\text{V}$, unless otherwise noted.

| PARAMETER | CONDITIONS | MIN | MAX | UNITS |
|------------------------------|--|-------|-----------|--------------------------------|
| Minimum Input Voltage | | | 2.3 | V |
| Quiescent Current | Not Switching $V_{\text{SHDN}} = 0.2\text{V}$ | | 36 0.5 | μA μA |
| FB Comparator Trip Voltage | V_{FB} Falling, $V_{\text{CTRL}} = 3.6\text{V}$ | 1.215 | 1.275 | V |
| FB Pin Bias Current | $V_{\text{FB}} = 1.25\text{V}$, $V_{\text{CTRL}} = 3.6\text{V}$ | | 30 | nA |
| FB Voltage Line Regulation | $2.3\text{V} < V_{\text{IN}} < 10\text{V}$ | | 0.1 | %/V |
| Switch Leakage Current | $V_{\text{SW}} = 36\text{V}$ | | 1 | μA |
| Switch Current Limit | | 85 | 140 | mA |
| Schottky Reverse Leakage | $V_{\text{CAP-SW}} = 36\text{V}$ | | 10 | μA |
| PNP Disconnect Q Current | $I_{\text{OUT}} = 0$, $V_{\text{CAP}} = 36\text{V}$ (Note 3) | | 5 | μA |
| PNP Disconnect Leakage | $\text{SHDN} = 0.2$, $V_{\text{CAP}} = 10\text{V}$, $V_{\text{OUT}} = 0\text{V}$ | | 5 | μA |
| PNP Disconnect Current Limit | $V_{\text{CAP}} = 10\text{V}$, $V_{\text{OUT}} = 0\text{V}$ | 25 | 75 | mA |
| SHDN Pin Current | $V_{\text{SHDN}} = 3.6\text{V}$ | | 10 | μA |
| SHDN Input Voltage High | | 2.3 | | V |
| SHDN Input Voltage Low | | | 0.2 | V |
| CTRL Pin Bias Current | $V_{\text{CTRL}} = 0.5\text{V}$, $V_{\text{FB}} = 1\text{V}$ | | 80 | nA |
| CTRL to FB Offset | $V_{\text{CTRL}} = 0.5\text{V}$ (Note 3) | | 7 | mV |

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Current consumed by Disconnect PNP when there is no load on the OUT pin.

Note 3: This figure is computed according to $((V_{\text{FB}} \text{ falling} + V_{\text{FB}} \text{ rising})/2) - V_{\text{CONTROL}}$.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-3464